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(54) Memory device

(57) A Magnetic Random Access Memory ("MRAM") device(100) includes an array (102) of memory cells (104). The device (100) generates reference signals that can be used to determine the resistance states of each memory cell in the array, despite variations in resistance due to manufacturing tolerances and other factors such as temperature gradients across the array, electromagnetic interference and aging.

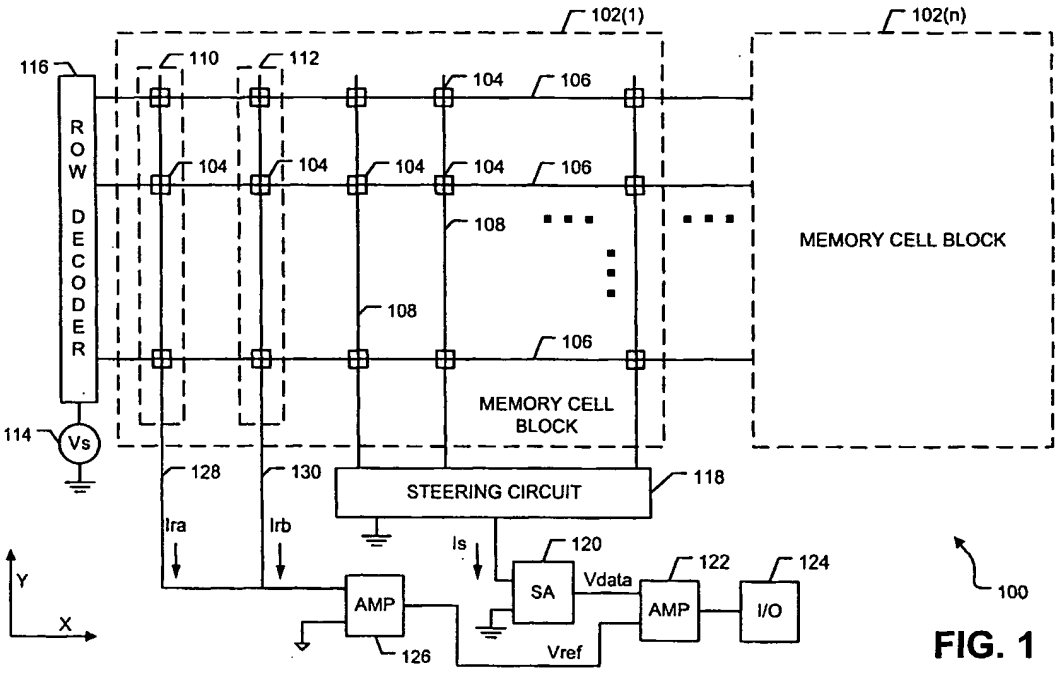

FIG. 1

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Description

[0001] The present invention relates to a memory device, for example a magnetic random access memory device including an array of memory cells and circuitry for sensing resistance states of the memory cells.

[0002] Magnetic Random Access Memory ("MRAM") is a non-volatile memory that is being considered for long-term data storage. Performing read and write operations in MRAM devices would be orders of magnitude faster than performing read and write operations in conventional long-term storage devices such as hard drives. In addition, the MRAM devices would be more compact and would consume less power than hard drives and other conventional long-term storage devices.

[0003] A typical MRAM device includes an array of memory cells. Word lines extend along rows of the memory cells, and bit lines extend along columns of the memory cells. Each memory cell is located at a cross point of a word line and a bit line.

[0004] A memory cell stores a bit of information as an orientation of a magnetization. The magnetization of each memory cell assumes one of two stable orientations, or states, at any given time. These two stable orientations, parallel and anti-parallel, may represent logic values of '0' and '1.'

[0005] The magnetization orientation affects the resistance of a memory cell. For instance, resistance of a memory cell is a first value R if the magnetization orientation is parallel, and the resistance of the memory cell is a second value $R+\Delta R$ if the magnetization orientation is anti-parallel. The magnetization orientation of a selected memory cell and, therefore, the logic state of the memory cell may be read by sensing the resistance state of the memory cell.

[0006] The resistance state of a selected memory cell may be read by applying a sense voltage to a word line crossing the selected memory cell and sensing a current on a bit line crossing the selected memory cell. The sense current (Is) is the ratio of the sense voltage (Vs) and the resistance of the selected memory cell (R or $R+\Delta R$). Thus, the sense current should be about equal to either $Is_0=Vs/R$ or $Is_1=Vs/(R+\Delta R)$. The sense current may be converted to a voltage. The resistance state of the selected memory cell may be determined by comparing the data voltage to a reference voltage (Vref). For example, the logic value stored in the selected memory cell is a logic '0' if the data voltage is greater than the reference voltage (that is, Vdata>Vref), and the logic value is a logic '1' if the data voltage is less than the reference voltage (that is, Vdata<Vref).

[0007] Generating reference signals for a large cross point resistive MRAM array is a complicated task. There is a loading effect of unselected memory cells. There are also "sneak paths" in the resistive array. Further, if manufacturing tolerances are not controlled adequately, there will be significant variations in memory cell resistances across the array. Consequently, a reference signal that is used by one group of memory cell might not be usable by another group of memory cells.

[0008] Generating the reference signals becomes increasingly complicated as device geometry is reduced. As the geometry is reduced, it becomes increasingly difficult to control manufacturing tolerances. Yet it is a goal of device manufacturers to decrease device geometry. Moreover, resistance variations can result from temperature gradients across the array, surrounding electromagnetic noise, and physical effects such as aging.

[0009] The present invention seeks to provide an improved memory device.

[0010] According to an aspect of the present invention, there is provided a memory device as specified in claim 1.

[0011] The preferred embodiment can provide a device which can provide a device which can establish reliable reference signals for the memory cells of an MRAM array.

[0012] An embodiment of the present invention is described below, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is an illustration of an embodiment of MRAM device;
Figure 2 is a flowchart of a read operation by the device shown in Figure 1;
Figure 3 is an illustration of another embodiment of MRAM device;
Figure 4 is a flowchart of a read operation by the device shown in Figure 3;
Figure 5 is an illustration of yet another embodiment of MRAM device;
Figure 6 is a timing diagram for the device shown in Figure 5;
Figure 7 is an illustration of still another embodiment of MRAM device; and
Figure 8 is a timing diagram for the device shown in Figure 7.

[0013] As shown in the drawings for purposes of illustration, there are described embodiments of MRAM device including an array of memory cells.

[0014] The circuit can generate reference signals that are usable by the memory cells in the array, despite variations in resistance due to manufacturing tolerances and other factors such as temperature gradients across the array, electromagnetic interference and aging. Four different MRAM devices will be described below. First and second MRAM devices 100 and 200, shown in Figures 1 and 3, include reference cells that are used to generate reference signals. Third and fourth MRAM devices 300 and 400, shown in Figures 5 and 7, include capacitors that are used to generate the reference signals.

Embodiment 1

[0015] Referring to Figure 1, the first MRAM device 100 includes an array of memory cells 104. The memory cells 104 are typically arranged in rows and columns, with the rows extending along an x-direction and the columns extending along a y-direction. The array may have any number of rows and columns of memory cells.

[0016] The memory cells 104 are organized in contiguous blocks 102(1) to 102(n). Figure 1 shows the first block 102(1) in some detail. Only a few rows and columns of memory cells 104 are shown. The n^{th} block 102 (n) is shown in phantom. Blocks 102(2) to 102(n-1) between the first and n^{th} blocks are not shown.

[0017] Word lines 106 extend along the x-direction in a plane on one side of the memory cell array 102. Bit lines 108 extend along the y-direction in a plane on another side of the memory cell array 102. Each memory cell 104 is located at the cross point of a word line 106 and a bit line 108.

[0018] Each memory cell 104 has two stable resistance states R_0 and R_1, where $R_0 \neq R_1$. For example, a first resistance state R_0 corresponds to the logic value '0' and a second resistance state R_1 corresponds to the logic value '1'. The resistance state of a selected memory cell 104 may be set by exposing the selected memory cell to external magnetic fields. The external magnetic fields may be generated by supplying write currents to the word and bit lines 106 and 108 crossing the selected memory cell 104.

[0019] Two columns 110 and 112 in each block are reserved as reference columns. Each reference cell 104 of the first reference column 110 always stores a logic '1' and each reference cell 104 of the second reference column 112 always stores a logic '0'. The memory cells 104 in the remaining columns of each block store user data. Each word line 106 crosses a row of memory cells 104 that store user data, as well as a memory cell 104 in the first reference column 110 and a memory cell 104 in the second reference column 112. Thus, each word line 106 crosses a row including a memory cell 104 that always stores a logic '0', a memory cell 104 that always stores a logic '1' and multiple memory cells 104 for storing user data. The memory cells 104 in the reference columns 110 and 112 have the same construction as the memory cells 104 that store user data.

[0020] Although the reference columns 110 and 112 are shown as being the first and second columns of the first block 102(1), they are not so restricted. The reference columns 110 and 112 may occupy any positions within a memory cell block 102.

[0021] The MRAM device 100 further includes a row decoder 116 for selecting a word line 106 during a read operation. The word line may be selected by applying a sense voltage Vs to it. The sense voltage may be provided by a voltage source 114.

[0022] The MRAM device 100 further includes a steering circuit 118 and a sense amplifier 120 for each block 102(j). Multiple bit lines 108 are connected to each steering circuit 118. Each steering circuit 118 includes a set of switches that connect a selected bit line to a sense input of the sense amplifier 120. Other unselected bit lines are connected to a ground potential. An output of the sense amplifier 120 is supplied to a second amplifier 122, which, in turn, is coupled to an I/O pad 124 of the MRAM device 100.

[0023] A half-gain amplifier 126 is also provided for each block 102(j). A reference input of the half-gain amplifier 126 is connected to a first bit line 128 crossing the memory cells 104 of the first reference column 112. The reference input of the half-gain amplifier 126 is also connected to a second bit line 130 crossing the memory cells 104 of the second reference column 114.

[0024] Additional reference is now made to Figure 2, which shows a flow chart 150 illustrating a read operation by the first MRAM device 100. At the beginning of the read operation, a word line 106 and a bit line 108 are selected (block 152). Selecting the word and bit line 106 and 108 causes a sense current Is to flow through the selected word and bit lines 106 and 108. The sense current Is also flows though the memory cell 104 at the cross point of the selected word and bit lines 106 and 108. For example, the row decoder 116 may select a word line 106 by applying a sense voltage Vs to that word line 106, and the steering circuit 118 may select a bit line 108 by applying a virtual ground potential to that bit line 108. Other unselected bit lines are connected to a ground potential by the steering circuit 118. The row decoder 116 and the steering circuit 118 make the selections in response to row and column addresses.

[0025] The sense current Is is supplied to the sense input of the sense amplifier 120. Magnitude of the sense current is inversely proportional to the resistance state (and, therefore, logic state) of the selected memory cell 104. The sense amplifier 120, which has a feedback resistor (Rf), converts the sense current Is to a data voltage Vdata. An output of the sense amplifier 120 provides the data voltage Vdata to an input of the second amplifier 122.

[0026] Applying a sense voltage Vs to the selected word line 106 also causes a first reference current Ira to flow through the memory cell 104 at the cross point of the selected word line 106 and the bit line 128 crossing the first reference column 110. Similarly, applying the sense voltage Vs causes a second reference current Irb to flow through the memory cell 104 at the cross point of the selected word line 106 and the bit line 130 crossing the second reference column 112. Thus, reference cells 104 in the reference columns 110 and 112 are selected when a word line 106 is selected. Because the reference cell 104 in the first reference column 110 stores the logic '1' (and therefore has a resistance R_1), the first reference current Ira equals Vs/R_1. Because the reference cell 104 in the second reference column 112 stores the logic '0' (and therefore has a resistance R_0), the second reference current Irb equals Vs/R_0.

[0027] The reference currents Ira and Irb are supplied to the reference input of the half-gain amplifier 126. The reference currents Ira and Irb are summed by the half-gain amplifier 126 (block 154), and the sum is halved and converted into a reference voltage Vref by the half-gain amplifier 126 (block 156). Thus, Vref = (Ira + Irb)Rf/2. An output of the half-gain amplifier 126 provides the reference voltage Vref.

[0028] The second amplifier 122 compares the data voltage Vdata to the reference voltage Vref. The comparison indicates whether the selected memory cell 104 stores a logic '1' or a logic '0' (block 158).

[0029] Using first and second reference columns 110 and 112 in each block is based on an assumption that variations in resistance values of the memory cells are a function of distance across the array. That is, memory cells 104 that are closer together will have less variation in resistance states than memory cells 104 that are farther apart. Thus, the first and second columns 110 and 112 of each memory cell block 102(j) (where $1 \leq j \leq n$) are localized with respect to memory cells 104 that store user data. Moreover, the reference cells in the reference cell columns 110 and 112 form a part of the memory cell block 102(j). Consequently, any variations in the word line 106 or loading effect of other unselected memory cells within the block 102(j) will have similar effects on the reference cells in the same block 102(j). Therefore, the selected memory cell and the reference cells in the reference cell columns 110 and 112 of the same block 102(j) tend to track one another for better common mode rejection of noise and temperature. Resulting is a more reliable determination of the resistance states of the selected memory cells.

Embodiment 2

[0030] Figure 3 shows the second memory device 200, which is similar to the first memory device 100. The second memory device 200 includes an array of memory cells 204, word lines 206 crossing rows of the memory cells 204 and bit lines 208 crossing columns of the memory cells 204. The memory cells 204 are organized in blocks 202(1) to 202(n). Only one block 202(j) is shown in Figure 3.

[0031] For each block 202(j) of the second device 200, there is a first pair of reference cells 251 and 252 connected in series and second pair of reference cells 253 and 254 connected in series. The first pair of reference cells 251/252 is connected in parallel to the second pair of reference cells 253/254. The reference cells 251/252 of the first pair always store a logic '0' and a logic '1' and have resistances of R_{0a} and R_{1a}, respectively. The reference cells 253/254 of the second pair always store a logic '0' and a logic '1' and have resistances of R_{0b} and R_{1b}, respectively. Thus, the combined resistance of Rref of the four reference cells 251, 252, 253 and 254 is about $(R_{0a}+R_{1a})(R_{0b}+R_{1b})/(R_{0a}+R_{1a}+R_{0b}+R_{1b})$. If $R_0=R_{0a}=R_{0b}$ and $R_1=R_{1a}=R_{1b}$, then $Rref = (R_0+R_1)/2$, whereby the reference resistance Rref is mid-way between the resistances R_0 and R_1.

[0032] The reference cells 251, 252, 253 and 254 are all made of the same material and all have the same size as the memory cells in their corresponding block 202(j). Moreover, the reference cells 251, 252, 253 and 254 are located in the vicinity of their corresponding block 202(j).

[0033] The reference cell pairs 251/252 and 253/254 are coupled between a row decoder 216 and a reference input of a sense amplifier 256. The row decoder 216 applies a sense voltage Vs to the reference cells 251, 252, 253 and 254 during a read operation on a selected memory cell within the block 202(j). A steering circuit 218 is coupled between the bit lines 208 and a sense input of the sense amplifier 256. An output of the sense amplifier is coupled to an I/O pad 224.

[0034] Additional reference is now made to Figure 4, which shows a flow chart 260 illustrating a read operation in the second MRAM device 200. At the beginning of the read operation, a word line 206 and a bit line 208 are selected (block 262), whereby the row decoder 216 applies a sense voltage Vs to the selected word line 206 and the steering circuit 218 connects the selected bit line 208 to the sense amplifier 256 and all unselected bit lines to ground. A sense current Is flows through a selected memory cell and the selected bit line to the sense input of the sense amplifier 256. At the same time, the row decoder 216 also applies a sense voltage Vs to the reference cell pairs 251/252 and 253/254 (block 264), whereby a reference current Ir flows to the reference input of the sense amplifier 256. The reference current Ir is equal to Vs/Rref.

[0035] The sense amplifier 256 compares the sense signal Is to the reference signal Ir. The comparison indicates whether the selected memory cell 204 stores a logic '1' or a logic '0' (block 266).

Embodiment 3

[0036] Figure 5 shows the third memory device 300, which includes an array of memory cells 304, word lines 306 crossing rows of the memory cells 304 and bit lines 308 crossing columns of the memory cells 304. Only a single memory cell block 302(j) is shown in Figure 5. The third memory device 300 further includes a steering circuit 318, a first amplifier 319, a sense (second) amplifier 320 and a sample and hold ("S/H") 321 for each memory cell block 302(j).

[0037] The steering circuit 318 couples a selected bit line to an input of the first amplifier 319 and it couples unselected bit lines of the memory cell block 302(j) to a ground potential. The S/H 321 includes a first capacitor 322 (which functions as data signal storage device), a second capacitor 324 (which functions as a first reference signal storage device) and a third capacitor 326 (which functions as a second reference signal storage

device). The first capacitor 322 is coupled to an output of the first amplifier 319 by a first switch 328. The second capacitor 324 is coupled to the first amplifier 319 by second and third switches 330 and 332. The third capacitor 326 is coupled to the steering circuit output by the third switch 332. The first capacitor 322 is coupled to a sense input of the sense amplifier 320. The second capacitor 322 is coupled to a reference input of the sense amplifier 320.

[0038] The S/H 321 is not necessarily local to the memory cells being sensed. The S/H 321 may be formed on a silicon substrate of the third device 300.

[0039] The S/H 321 further includes control logic 334 for the switches 328, 330 and 332. The control logic 334 controls the switches 328, 330 and 332 during a read operation on a selected memory cell, as indicated in Figure 6.

[0040] Each block 302(j) of the third device 300 also includes a write circuit 336. During a write operation on a selected memory cell, the write circuit 336 applies a first write current to the selected word line and a second write current to the selected bit line. All other lines are left unconnected. Each write current produces a magnetic field at the selected memory cell. The combined magnetic fields set the selected memory cell to the low resistance state R_0 or the high resistance state R_1, depending upon the write current direction on the bit line 308. Although the read and write circuits are shown as separate circuit, they may be integrated.

[0041] Reference is now made to Figure 6. At time T0, a word line 306 and a bit line 308 are selected, whereby a sense signal flows through a selected memory cell 304. Magnitude of the sense signal depends upon the resistance state of the selected memory cell 304. At time T0, all three switches 328, 330 and 332 are open.

[0042] Immediately following time T0, the first switch 328 is closed to allow the first amplifier 319 to charge the first capacitor 322 to a voltage Vdata. At time T1, the first switch 322 is opened. The voltage Vdata at time T1 represents the resistance state of the selected memory cell 304.

[0043] At time T1, a logic '0' is written to the selected memory cell 304. Thus, the resistance of the selected memory cell 304 is set to R_0.

[0044] At time T2, the selected memory cell 304 is read again by selecting the crossing word and bit lines 306 and 308. Consequently, a sense signal flows through the selected memory cell 304.

[0045] After time T2, the second and third switch 330 and 332 are closed to allow the second and third capacitors 324 and 326 to charge to voltage V_0. The voltage V_0 at time T3 represents a logic '0' stored in the selected memory cell 104.

[0046] At time T3, the second and third switches 330 and 332 are opened. and a logic '1' is written to the selected memory cell 304. Thus, the resistance of the selected memory cell is set to R_1.

[0047] At time T4, the selected memory cell 304 is read again by selecting the crossing word and bit lines 306 and 308. Consequently, a sense signal flows through the selected memory cell 304.

[0048] After time T4, the third switch 332 is closed to charge the third capacitor 326 to voltage V_1. At time T5, the third switch 332 is opened. The voltage V_1 at time T5 represents a logic '1' stored in the selected memory cell 304.

[0049] After time T5, the second switch 330 is closed, thereby allowing the charge on the second capacitor 324 and the charge on the third capacitor 326 to equalize to a reference voltage Vref. The transfer of charge between the second and third capacitors 324 and 326 can occur very quickly.

[0050] At time T6, the reference voltage Vref is available to the reference input of the sense amplifier 320. The voltage Vdata on the first capacitor 322 is applied to the sense input of the sense amplifier 320. The sense amplifier 320 compares the voltage Vdata to the reference voltage Vref to determine whether a logic '0' or a logic '1' was stored in the selected memory cell.

[0051] At time T7, the logic value is restored to the selected memory cell 304. Thus, if a logic '0' was sensed, the write circuit 336 writes a logic '0' to the selected memory cell 304. If a logic '1' was sensed, the write circuit 336 writes a logic '1' to the selected memory cell 304.

Embodiment 4

[0052] Figure 7 shows the fourth memory device 400, which is identical to the third memory device 300, except for the S/H 421. The S/H 421 of the fourth device 400 includes a first capacitor 422 (which functions as a data storage device), a second capacitor 424 (which functions as a first reference signal storage device), and a third capacitor 426 (which functions as a second reference signal storage device).

[0053] The first capacitor 422 is coupled to the first amplifier output by a first switch 428. The second capacitor 424 is coupled to the first amplifier output by a second switch 430. The third capacitor 426 is coupled to the first amplifier output by a third switch 432. A fourth switch 434 couples the second capacitor 424 to the third capacitor 426.

[0054] The first capacitor 422 is connected to a sense input of the sense amplifier 320. The third capacitor 426 is connected to the reference input of the sense amplifier 320.

[0055] The S/H 421 further includes control logic 436 for controlling the switches 428, 430, 432 and 434 during a read operation on a selected memory cell 304. Control of the switches 428, 430, 432 and 434 is illustrated in Figure 8.

[0056] Reference is now made to Figure 8. At time T0, a word line 306 and a bit line 308 are selected, whereby a sense signal flows through a selected memory cell 304. Magnitude of the sense signal depends upon the

resistance state of the selected memory cell 304. At time T0, all four switches 428, 430, 432 and 434 are open.

[0057] Immediately following time T0, the first switch 428 is closed to allow the sense current to charge the first capacitor 422 to a voltage Vdata.

[0058] At time T1, the first switch 428 is opened. The voltage Vdata at time T1 represents the resistance state of the selected memory cell 304.

[0059] Also at time T1, a logic '0' is written on the selected memory cell 304. Thus, the resistance of the selected memory cell 304 is set to R_0.

[0060] At time T2, the selected memory cell 304 is read again by selecting the crossing word and bit lines 306 and 308. Consequently, a sense signal flows through the selected memory cell 304.

[0061] Following time T2, the second switch 430 is closed to allow the second capacitor 424 to charge to voltage V_0.

[0062] At time T3, the second switch 430 is opened, and a logic '1' is written to the selected memory cell 304. Thus, the resistance of the selected memory cell 304 is set to R_1.

[0063] At time T4, the selected memory cell 304 is read again by selecting the crossing word and bit lines 306 and 308. Consequently, a sense signal flows through the selected memory cell 304.

[0064] Following time T4, the third switch 432 is closed to allow the third capacitor 426 to charge to voltage V_1. At time T5, the third switch 432 is opened.

[0065] Following time T5, the fourth switch 434 is closed, thereby allowing the charge on the second capacitor 424 and the charge on the third capacitor 426 to equalize to a reference voltage Vref. The equalized voltage Vref is about midway between V_0 and V_1. That is, $Vref \approx (V_0+V_1)/2$. The reference voltage Vref is applied to the reference input of the sense amplifier 320.

[0066] At time T6, the reference voltage Vref is available to the reference input of the sense amplifier 320. The sense amplifier 320 compares the voltage Vdata on the first capacitor 422 to the reference voltage Vref to determine whether the selected memory cell 304 stored a logic '0' or a logic '1'. At time T7, the sensed logic value of the selected memory cell is restored to the selected memory cell.

[0067] Thus disclosed are MRAM devices that generate usable reference signals, despite variations in resistance due to manufacturing tolerances and other factors such as temperature gradients across the array, electromagnetic interference and aging. The first and second devices can perform read operations faster than the third and fourth devices. However, the third and fourth devices have much more robust reference signals to determine the logic states of selected memory cells because the reference signals are derived from the selected memory cells.

[0068] The signal storage devices in Figures 5 and 7 are not limited to capacitors. For example, the signal storage devices may be digital counters

[0069] The memory cells are not limited to any particular type. For example, the memory cells may be, without limitations, spin dependent tunneling ("SDT") junction devices or giant magnetoresistance ("GMR") devices.

[0070] The sense amplifiers are not limited to any particular type. Exemplary sense amplifiers are disclosed in assignee's copending patent applications U.S. serial no. 09/564308 filed May 03, 2000 (Attorney Docket No. 10990673-1) and U.S. serial no. 09/430,611 filed October 29. 1999.

[0071] Although several specific embodiments of the present invention have been described and illustrated, the present invention is not limited to the specific forms or arrangements of parts so described and illustrated.

[0072] Other embodiments will be apparent to the skilled reader from the teachings herein.

[0073] The disclosures in United States patent application no. 09/598,671, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

Claims

1. A memory device (100) including:

   a block (102) of memory cells (104);
   a first storage device (110) for storing a logic '1';
   a second storage device (112) for storing a logic '0';
   a sense amplifier (120); and
   a circuit (126) for generating a reference signal (Vref) for the sense amplifier by combining outputs of the first and second storage devices.

2. A device as in claim 1, wherein the first storage device includes a first group (11) of reference cells for the memory cells in the block; the second storage device includes a second group (112) of reference cells for the memory cell block; and wherein the circuit is operable to generate the reference signal by combining the outputs from the first and second reference cell groups; the first and second groups being local to the block of memory cells.

3. A device as in claim 2, wherein the first group includes a first column (110) of first reference cells and the second group includes a second column (112) of second reference cells; wherein each memory cell in the array is crossed by a word line (106), each word line also crossing a first reference cell in the first reference cell group and a second reference cell in the second reference cell column, whereby selection of a word line results in a corresponding pair of first and second reference cells being selected, outputs of the selected reference cell pair being combined by the circuit to generate the

reference signal.

4. A device as in claim 3, wherein a first bit line (128) crosses the first reference cells in the first column; wherein a second bit line (130) crosses the second reference cells in the second column; and wherein the circuit includes a half gain amplifier (126) having inputs coupled to the first and second bit lines.

5. A device (200) as in claim 2, wherein the first group includes a first reference cell (252) for storing a logic '1' and the second group includes a second reference cell (251) for storing a logic '0'; wherein the first and second reference cells are crossed by a trace; and wherein the circuit includes amplifier (256) having an input coupled to the trace.

6. A device as in claim 5, including an additional first reference cell (254) for storing a logic '1', an additional second reference cell (253) for storing a logic '0', and an additional trace crossing the additional reference cells; and wherein the additional trace is also coupled to the amplifier input.

7. A device as in claim 2, including an additional first reference cell group, an additional second reference cell group, an additional circuit and an additional sense amplifier for each additional block (102 (2)) to (102(n)) of memory cells in the array, wherein each additional first reference cell group includes first reference cells for storing a logic '1', each additional second reference cell group includes second reference cells for storing a logic '0', and each additional circuit is operable to generate a reference signal for a corresponding sense amplifier by combining outputs of corresponding first and second reference cell groups; and wherein each additional group of reference cells is local to its corresponding memory cell block.

8. A device (300) as in claim 1, including a third storage device (322); and wherein the circuit (321) includes first, second and third switches (328, 330 and 332) and control logic (334) for controlling the switches, the control logic being operable to cause the first switch to connect the selected memory cell to the third storage device during a first time interval, to cause the second and third switches to connect the first and second storage devices (326 and 324 to the selected memory cell during a second time interval, to cause the second switch to connect the selected memory cell to the third switch to equalize signals stored in the first and second storage devices, the equalized signal being the reference signal.

9. A device (400) as in claim 1, including a third storage device (428) for storing a logic value of a selected memory cell in the array; and wherein the circuit (421) includes first, second, third and fourth switches (428, 430, 432 and 434) and control logic (436) for controlling the switches, being operable to cause the first switch (428) to connect the selected memory cell to the third storage device (422) during a first time interval, to cause the second switch (430) to connect the first storage device (424)to the selected memory cell during a second time interval, to cause the third switch (432) to connect the selected memory cell to the second storage device (424) during a third time interval, and to cause the fourth switch (434) to equalize signals stored in the first and second storage devices during a fourth interval, the equalized signal being the reference signal.

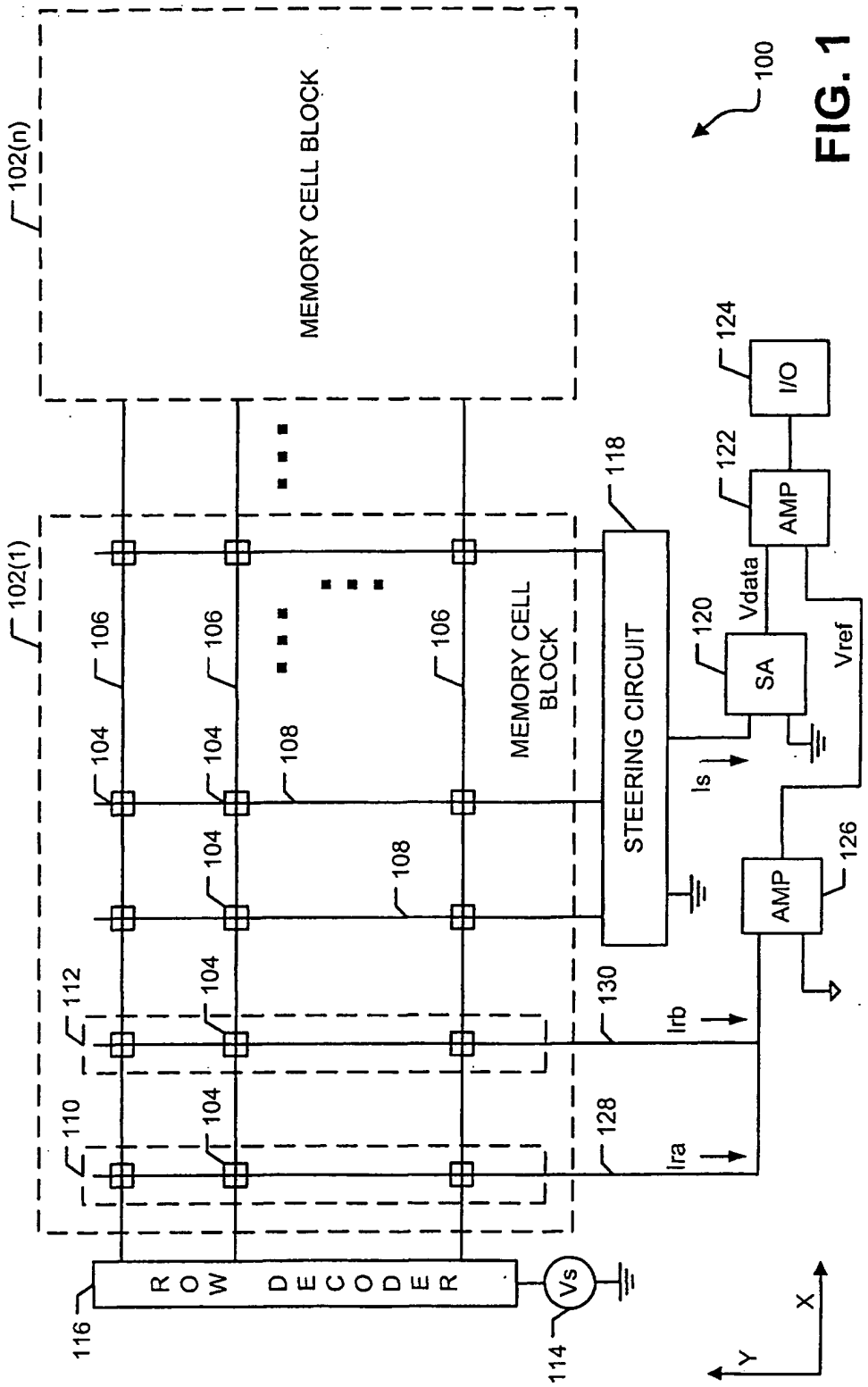

100
102(n)
MEMORY CELL BLOCK
102(1)
MEMORY CELL BLOCK
106
104
108
112
110
118
STEERING CIRCUIT
120
SA
Vdata
122
AMP
124
I/O
Vref
126
AMP
130
Irb
128
Ira
Is
ROW DECODER
116
Vs
114
Y
X

FIG. 1

FIG. 4

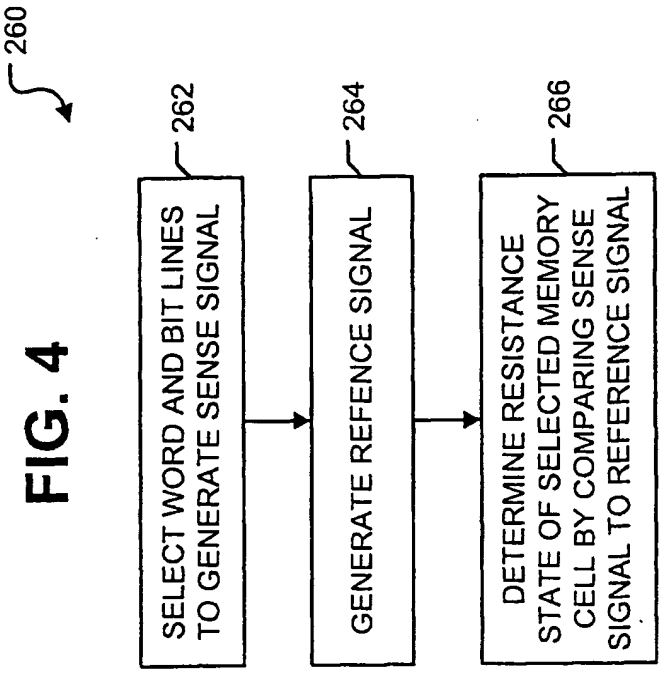
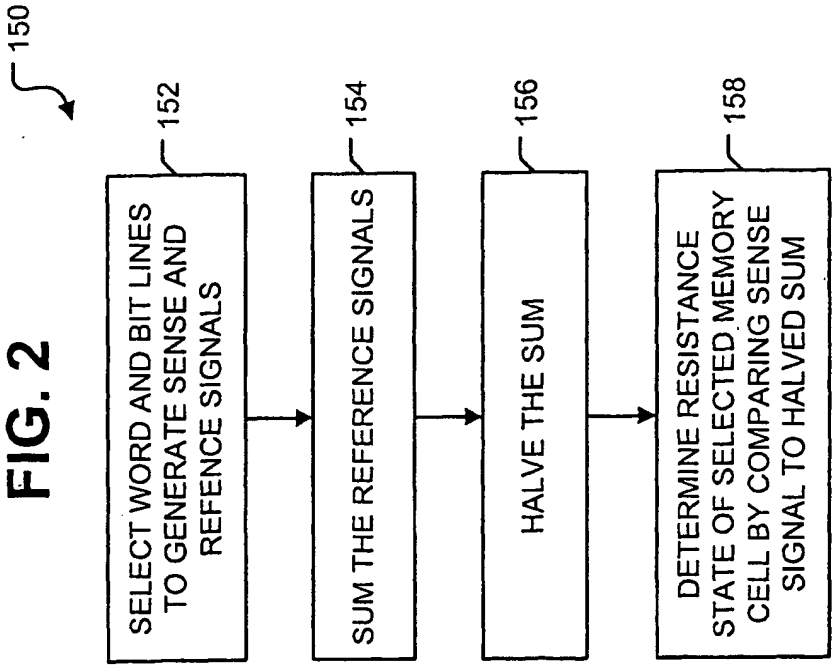

260
262
SELECT WORD AND BIT LINES TO GENERATE SENSE SIGNAL
264
GENERATE REFENCE SIGNAL
266
DETERMINE RESISTANCE STATE OF SELECTED MEMORY CELL BY COMPARING SENSE SIGNAL TO REFERENCE SIGNAL

FIG. 2


150
152
SELECT WORD AND BIT LINES TO GENERATE SENSE AND REFENCE SIGNALS
154
SUM THE REFERENCE SIGNALS
156
HALVE THE SUM
158
DETERMINE RESISTANCE STATE OF SELECTED MEMORY CELL BY COMPARING SENSE SIGNAL TO HALVED SUM

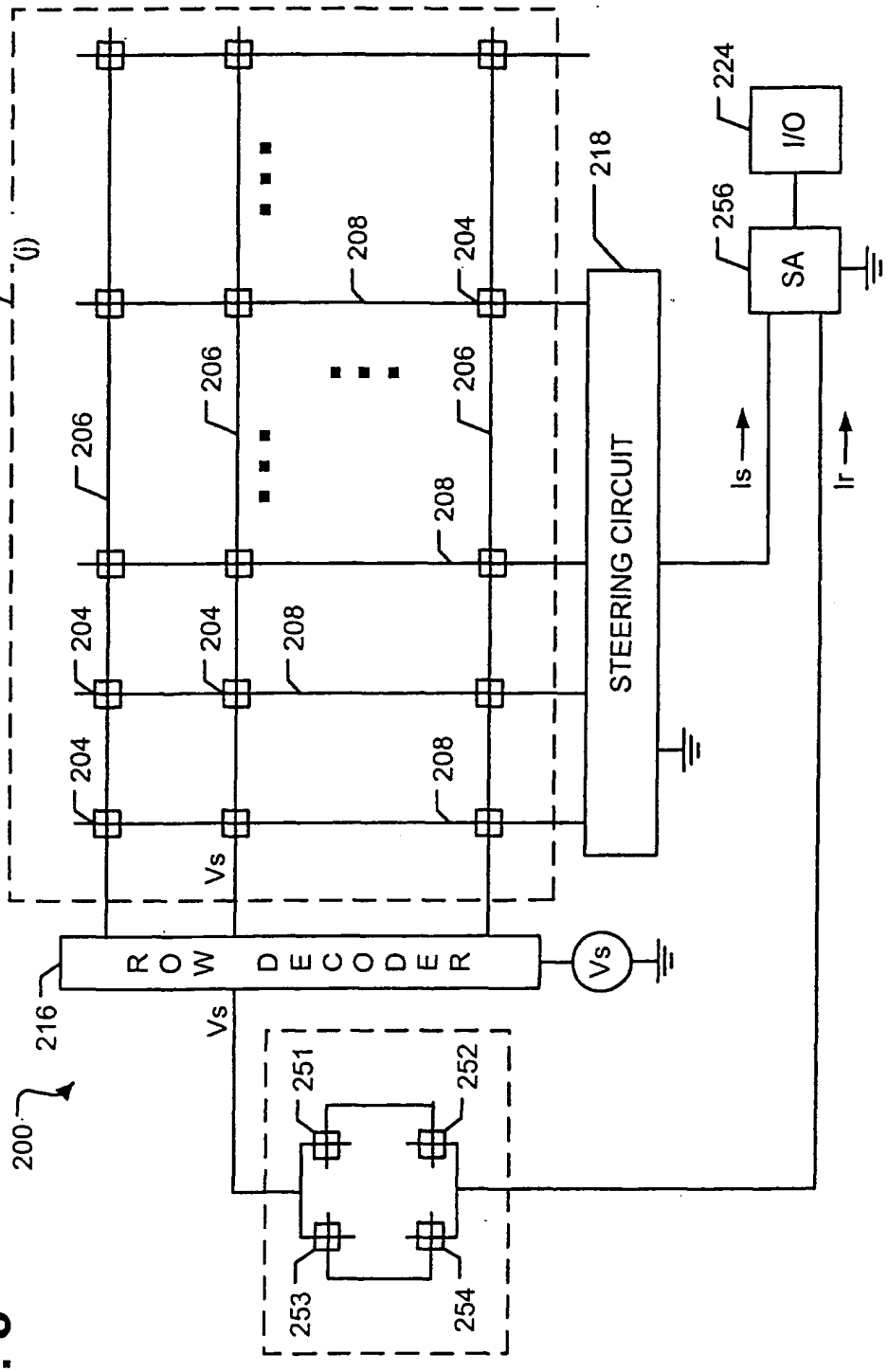

202
(j)
206
204
208
218
224
I/O
256
SA
STEERING CIRCUIT
Is
Ir
Vs
ROW DECODER
216
200
251
252
253
254

FIG. 3

FIG. 5

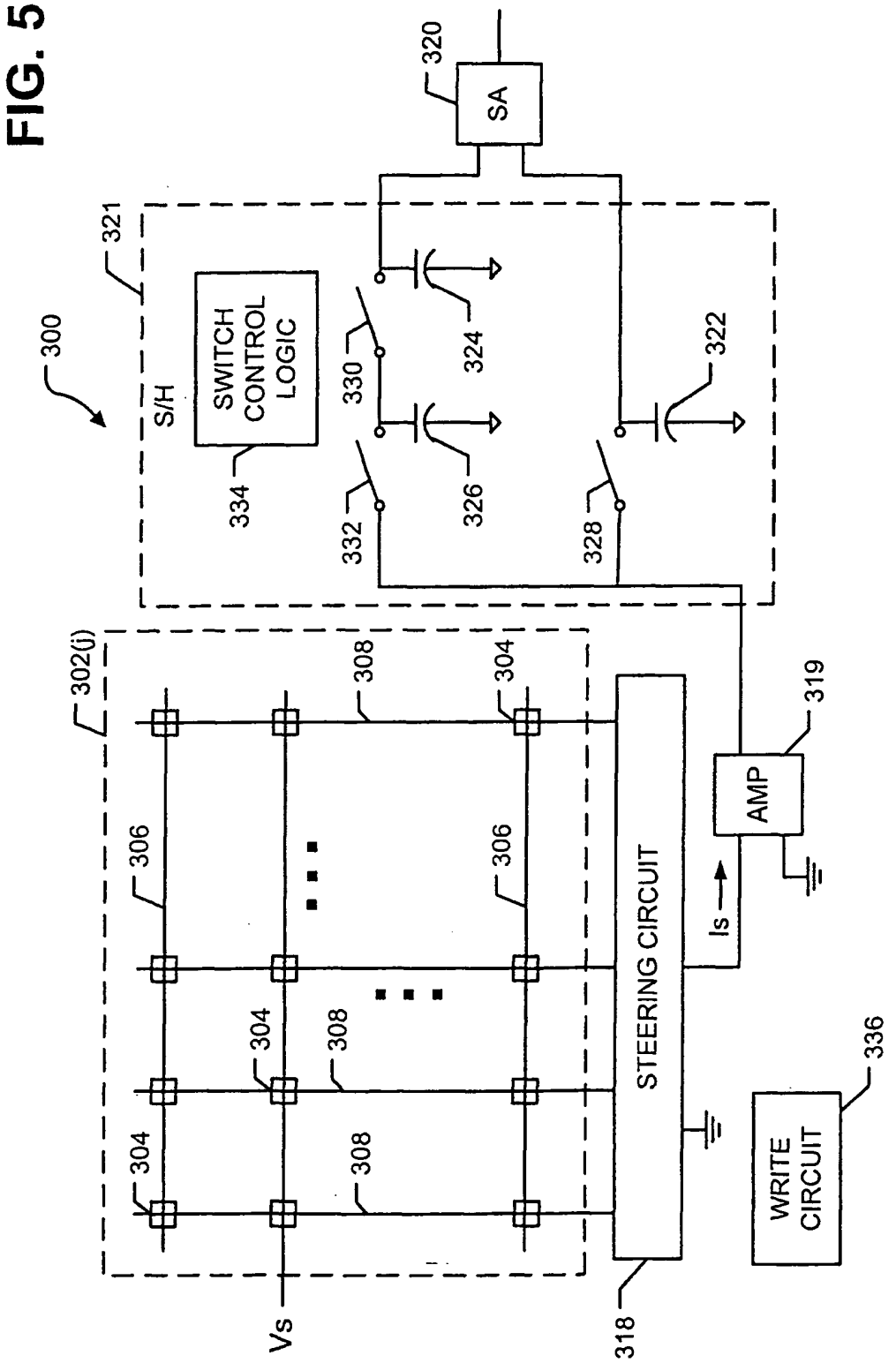

300
321
S/H
SWITCH CONTROL LOGIC
334
320
SA
322
324
326
328
330
332
302(j)
304
306
308
Vs
318
STEERING CIRCUIT
AMP
319
Is
336
WRITE CIRCUIT

FIG. 6

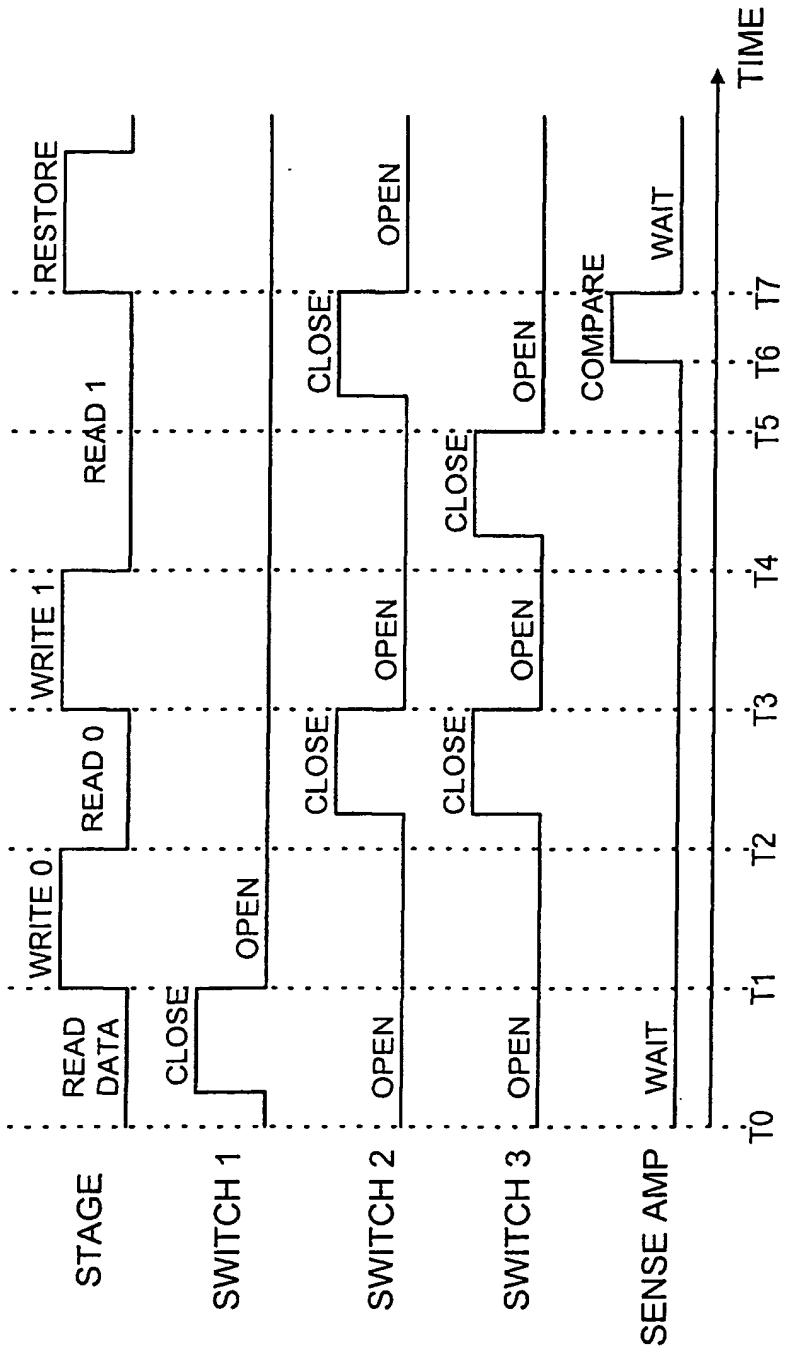

STAGE
SWITCH 1
SWITCH 2
SWITCH 3
SENSE AMP
TIME
T0
T1
T2
T3
T4
T5
T6
T7
READ DATA
WRITE 0
READ 0
WRITE 1
READ 1
RESTORE
CLOSE
OPEN
CLOSE
OPEN
CLOSE
OPEN
CLOSE
OPEN
WAIT
COMPARE
WAIT

FIG. 7

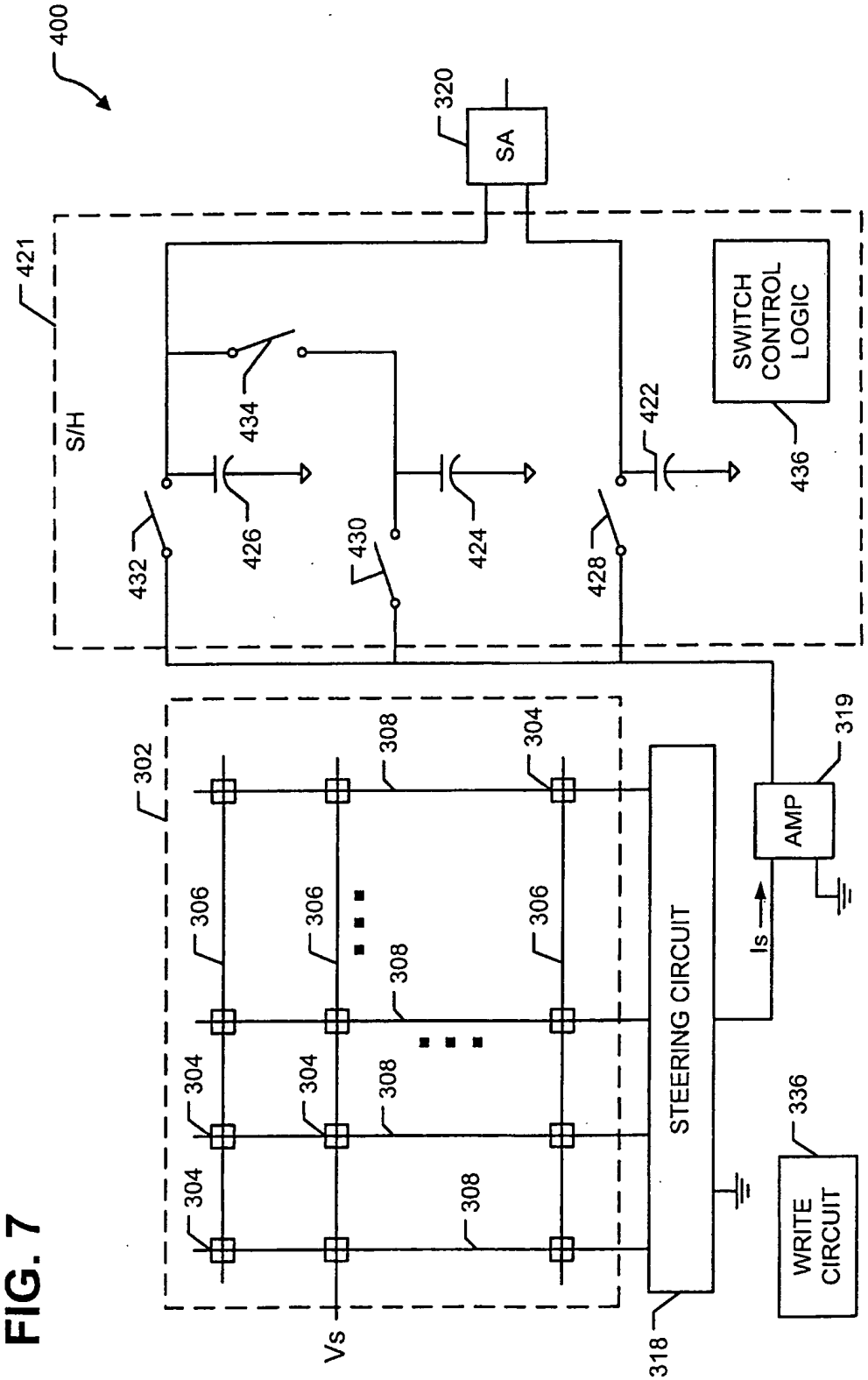
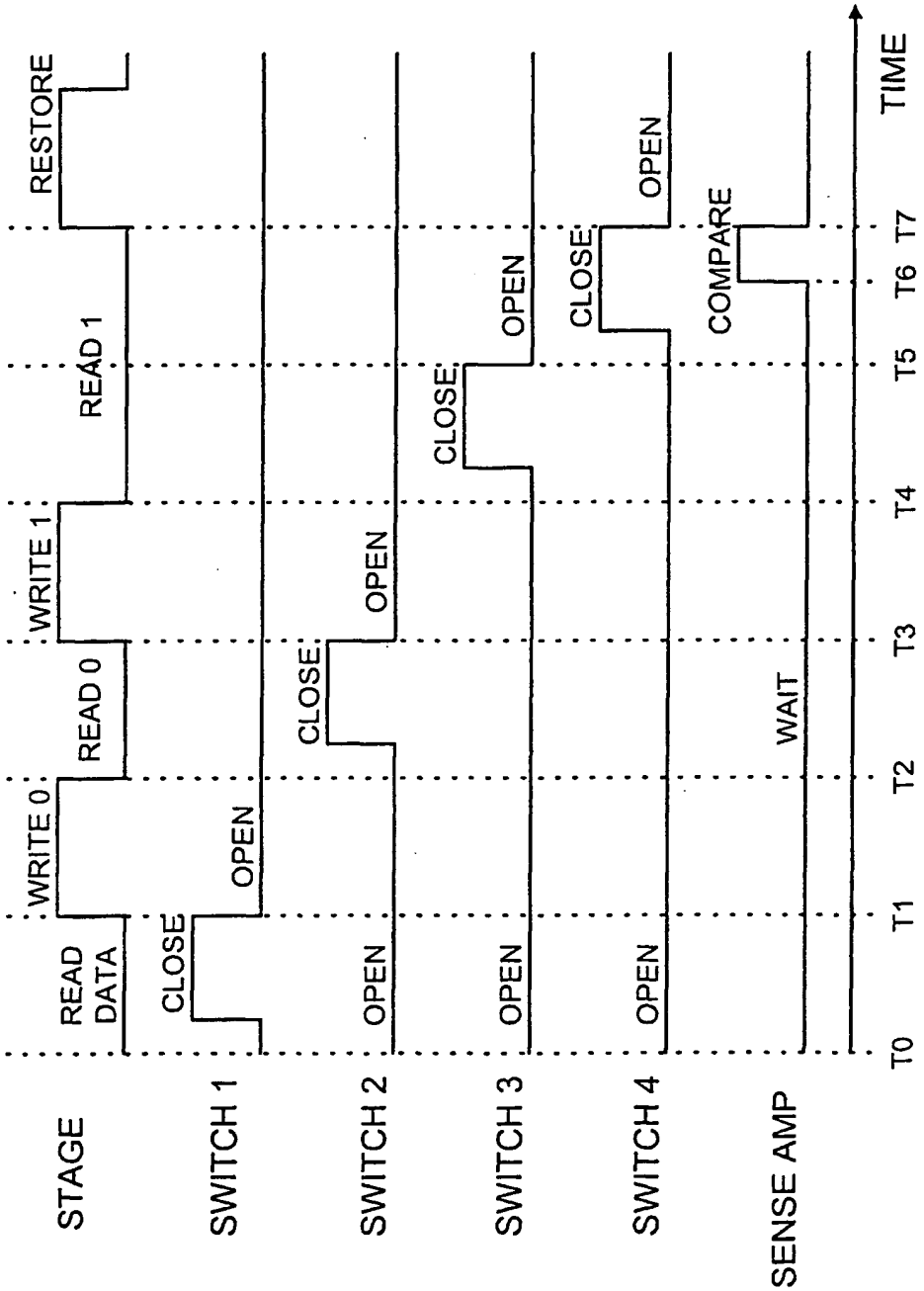

400
320
SA
421
S/H
SWITCH CONTROL LOGIC
434
422
436
426
430
424
432
428
302
308
304
319
AMP
306
Is
STEERING CIRCUIT
336
WRITE CIRCUIT
Vs
318

FIG. 8


STAGE
SWITCH 1
SWITCH 2
SWITCH 3
SWITCH 4
SENSE AMP
READ DATA
WRITE 0
READ 0
WRITE 1
READ 1
RESTORE
CLOSE
OPEN
WAIT
COMPARE
TIME
T0
T1
T2
T3
T4
T5
T6
T7

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 30 5342

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Place of search	Date of completion of the search	Examiner
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